

In the Claims:

1. (Original) A content addressable memory (CAM) device, comprising:
CAM logic that is configured to pass an instruction received at an instruction input port to an instruction output port without inspection or alteration so that the CAM device may be operated within a cascaded chain of CAM devices that collectively form multiple databases within a lookup engine.
2. (Original) The CAM device of Claim 1, wherein said CAM logic comprises:
an input instruction register that is configured to latch the instruction received at the instruction input port; and
an output instruction register that is configured to latch the instruction received from the input instruction register.
3. (Original) The CAM device of Claim 2, wherein said CAM logic further comprises an instruction FIFO that is configured to buffer instructions received from the input instruction register.
4. (Original) An integrated circuit system, comprising:
a cascaded chain of CAM devices that is configured to support passing of instructions down the cascaded chain without inspection or alteration using a distributed control architecture.
5. (Original) The system of Claim 4, wherein the CAM devices in said cascaded chain are arranged in a high-to-low CAM priority sequence.

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